REMARKS

Status of Claims:

Claims 1-3 and 10 are cancelled. New claims 11-19 are added. Thus, claims 4-9 and 11-19 are present for examination.

Allowable Subject Matter:

Applicant expresses appreciation to the Examiner for the indication that claim 9 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Objections:

Claims 1-4, 9, and 10 are objected to because of the formalities listed on page 2 of the Office Action.

Claims 1-3 and 10 have been cancelled.

Claim 4 has been amended to be independent and has been amended in accordance with the Examiner's suggestions, except that the "and" that was on line 15 has not been deleted because it is a transition between the "wherein" clauses.

Claim 9 has been amended in accordance with the Examiner's suggestion.

Claim Rejection:

Claims 1-8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (hereinafter AAPA) in view of Ishikura (U.S. Patent No. 6,421,816 B1) (hereinafter Ishikura).

Claims 1-3 and 10 have been cancelled. With respect to claims 4-8, as amended, the rejection is respectfully traversed.

Independent claim 4, as amended, recites a master slice semiconductor integrated circuit, comprising:

at least two wiring layers for wiring; and

a plurality of clock buffers connected by clock wirings in a form of a clock tree having at least two cascaded stages to distribute clock signals to a plurality of sequential circuits;

wherein each of said clock wirings among said plurality of clock buffers comprises a wiring layer switching portion which switches a clock wiring from a lower wiring layer of said at least two wiring layers to an upper wiring layer of said at least two wiring layers and then switches said clock wiring from said upper wiring layer to said lower wiring layer;

wherein said wiring layer switching portion comprises:

an output wiring which is formed of said lower wiring layer and connects one end thereof to a clock output of a clock buffer of a former stage;

an output side via wiring which connects one end thereof to the other end of said output wiring and connects the other end thereof to said upper wiring layer;

an input wiring which is formed of said lower wiring layer and connects one end thereof to a clock input of a clock buffer of a later stage; and

an input side via wiring which connects one end thereof to the other end of said input wiring and connects the other end thereof to said upper wiring layer; and

wherein said upper wiring layer is a wiring layer for **customized** wirings, and said lower wiring layer is a wiring layer for fixed wirings." (Emphasis Added).

Neither AAPA nor Ishikura, alone or in combination, disclose or suggest a mater slice semiconductor integrated circuit including the above-quoted features. The Examiner states that FIG. 15(a) to FIG. 15(d) of Ishikura "shows and teaches that the upper wiring layer is a wiring layer for **customized** wirings, and the low wiring layer is a wiring layer for fixed wirings". (Office Action; page 4) (Emphasis Added). In Ishikura, the description relating to these figures is made in column 15, line 22 to column 16, line 25. As is apparent from the description related to the figures, Ishikura neither discloses nor suggests that the upper wiring layer is a wiring layer for **customized** wirings. Moreover, AAPA does not cure the deficiency with respect to the teaching of Ishikura, because AAPA similarly does not disclose an upper wiring layer that is a wiring layer for customized wirings.

Therefore, independent claim 4, as amended is neither disclosed nor suggested by AAPA and the Ishikura reference and, hence, is believed to be allowable. The Patent Office has not made out a *prima facie* case of obviousness under 35 U.S.C. 103.

The dependent claims are deemed allowable for at least the same reasons indicated above with regard to the independent claims from which they depend.

New claims 11-19 recite features not found in either of AAPA or the Ishikura reference.

Conclusion:

Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741.

If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

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